REMARKS

The Final Office Action dated August 21, 2007 has been received and carefully noted. Claims 1-27 are currently pending in the subject application and claims 8-19 and 25-27 are presently under consideration. Claims 8-19 and 25-27 were rejected under 35 U.S.C. §103. No claims have been amended and claims 28-29 have been added. Support for the new claims can be found in at least paragraphs 0027-0029 of the Specification. A listing of claims can be found on pgs. 2-6 of this Reply.

Favorable reconsideration of the pending claims is respectfully requested in view of the comments herein.

I. Rejection of Claims 8 and 25 Under 35 U.S.C. §103(a)

Claims 8 and 25 stand rejected under 35 U.S.C. §103(a) as being anticipated by Good *et al.* (US 6,240,095 B1), in view of Shimojo *et al.* (US 5,787,072). It is requested that this rejection be withdrawn for at least the following reason. To establish a *prima facie* case of obviousness, the Examiner must show that the cited references, combined, teach or suggest each of the elements of the claims. Good *et al.* and Shimojo *et al.*, alone or in combination, do not teach or suggest all the claim limitations.

In particular, independent claims 8 and 25 recite: "***communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits***" (emphasis added).

The Examiner contends that Good *et al.* teaches such aspect by equating: (1) the "I/O controller" recited in independent claims 8 and 25 with the network interface circuit and (2) the "chipset" recited in independent claims 8 and 25 with the remote network device (*See* Final Office Action dated August 21, 2007, pg. 3 and Good *et al.*, Figure 1). However, this interpretation fails to teach the cited limitation because the remote network device is located in a ***separate computer*** from the network interface circuit (*See e.g.*, "remote server" of Good *et al.*, col. 3, line 66 – col. 4, line 2) and is not "within a device coupled to the I/O controller within the device," as recited in independent claims 8 and 25.

The Examiner responds, "Good is merely giving an example of a network device when stating at [*sic*] the network device can be a remote server. Good states that modifications and variations of the preferred embodiment are still within the scope of the invention (Good; Col 6

Lines 45-49), meaning the example given is not limiting. Nowhere does Good teach the network device being away from the network interface card as suggested by applicant" (*See* Final Office Action dated August 21, 2007, pg. 2). The Applicants respectfully disagree with such reasoning.

While the identification of the "network device" as a "remote server" in Good *et al.* was presented in the form of an example (*See* Good *et al.*, Figure 1 and col. 3, line 66 – col. 4, line 2), the cited reference fails to present any other explanation or example that might indicate another interpretation or configuration. Although some modifications and variations of Good *et al.* may still fall within the scope of the invention, they must be apparent to those of ordinary skill in the art (*See Id.* at col. 6, ll. 46-49)—such as varying "the size of the various input, output, command and receive buffers … according to the anticipated need for the buffer memory interface" (*See Id.* at col. 6, ll. 49-56). Good *et al.* must still ***teach or suggest*** all the claimed limitations; but based on the visual orientation of the items shown in Figure 1 (*See Id.* at Figure 1, Item 16) and the sole example specified, the cited reference is silent regarding "***communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits***" (*See* independent claims 8 and 25) (emphasis added).

The Examiner further contends, "As applicant has not defined the term 'device,' the Examiner has given the term its broadest reasonable interpretation. Using this interpretation, the whole system of Good can be considered a device" (*See* Final Office Action dated August 21, 2007, pg. 2). The Applicants aver to the contrary.

As interpreted by a person having ordinary skill in the art, "In the context of computer technology, a device is ***a unit*** of hardware" (*See* device – a definition from Whatis.com. [Online] Available http://whatis.techtarget.com/definition/0,,sid9_gci211937,00.html, Last updated on July 25, 2001) (emphasis added) and may also be described as those units "separately installable and replaceable" (*See Id.*). Accordingly, a person having ordinary skill in the art would not consider the three items illustrated in Figure 1—"the buffer memory interface … interposed between a network device … and a host device" (*See* Good *et al.*, Figure 1 and col. 3, line 66 – col. 4, line 2)—to entirely be one single device. Rather, they would likely be considered at least three separate devices. Therefore, Good *et al.* fails to disclose "***communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits***" (emphasis added) as recited in independent claims 8 and 25.

The Examiner has not relied upon and the Applicants are unable to discern any part of Shimojo *et al.* that teaches the limitations discussed above. Thus, Shimojo *et al.* fails to cure the aforementioned deficiencies regarding independent claims 8 and 25. For at least these reasons, it is readily apparent that Shimojo *et al.* and Good *et al.*, alone or in combination, do not teach or suggest independent claims 8 and 25. The Applicants request that this rejection be withdrawn.

II. Rejection of Claims 9, 12-19, and 26-27 Under 35 U.S.C. §103(a)

Claims 9, 12-19, and 26-27 stand rejected under 35 U.S.C. §103(a) as being anticipated by Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* (US 2002/0150049 A1). This rejection should be withdrawn for at least the following reason. Claims 9 and 12-19 depend from independent claim 8 and claims 26-27 depend from independent claim 25. The Examiner has not relied upon and the Applicants are unable to discern any part of Collier *et al.* that discloses "communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits" as recited in independent claims 8 and 25. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest claims 9, 12-19, and 26-27. Accordingly, it is respectfully requested that this rejection be withdrawn.

III. Rejection of Claims 10-11 Under 35 U.S.C. §103(a)

Claims 10-11 stand rejected under 35 U.S.C. §103(a) as being anticipated by Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* and Anderson (US 2003/0223369 A1). It is requested that this rejection be withdrawn for at least the following reason. Claims 10-11 depend from independent claim 8. The Examiner has not relied upon and the Applicants are unable to discern any part of Anderson that cures the aforementioned deficiencies regarding independent claim 8. Thus, it is readily apparent that Good *et al.*, Shimojo *et al.*, Collier *et al.*, and Anderson, alone or in combination, do not teach or suggest claims 10-11; the Applicants request that this rejection be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all claims presently under consideration patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Lori Ciccio 10/10, 2007